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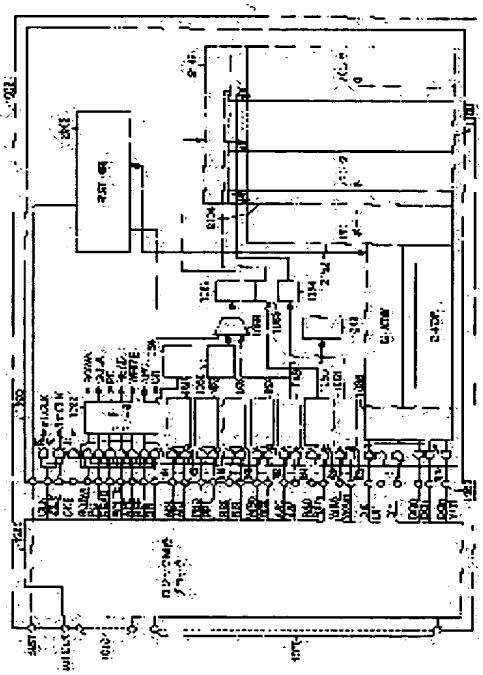
(71)Applicant : MITSUBISHI ELECTRIC CORP
(72)Inventor : OISHI TSUKASA
HIDAKA HIDETO

(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor integrated circuit device, provided with a built-in test circuit, with which a defective memory cell can be replaced by a redundant memory cell.
SOLUTION: After data has been written in a memory cell array according to an internal address signal, in read-out operation, read-out data from each memory cell is compared with expected value data. A row decoder 2142 selects plural memory cells, belonging to the same row of the memory cell array en bloc according to the address signal. A BIST circuit 2002 discriminates carrying out of relieving in a spare memory cell row, rather than in a spare memory cell column, when plural defective memory cells are detected in plural memory cells selected en bloc.



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